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REALIZATION OF 1=2 TERNARY LOGIC GATES (BUILDING BLOCK) USING MOSFET

VIRANG JHAVERI, YASH JAIN, SHANAY KOTHARI & VISHESH KAMDAR

Student, D. J. Sanghvi College of Engineering, Mumbai, Maharashtra, India

ABSTRACT

In this paper, we discuss the practical realization of 1=2 Logic gates using MOSFET. The 1=2 logic gate design is a hitherto unimplemented and unused design. Current circuitry based on the logic of aforementioned gates is complex since it uses registers and counters. The present CMOS technology does not use depletion mode transistors. The prime objective in our work is to minimize the number of transistors used, eliminate the use of resistors to lower the power consumption, reduce the propagation delay time and eliminate depletion mode transistors. The reduction in the number of transistors is main focus as that enabled a more compact design which utilized the less chip area.

KEYWORDS: 1=2 Logic Gates, Basic Gates, Integrated Circuit, MOSFET, Multi-Valued Logic Design, Ternary Logic

INTRODUCTION

Ternary based logic gives us new and exciting possibilities in gate design. The traditional binary based gate design gives us a single unary operator gate and three binary operator gates (with their corresponding negations. Whereas, ternary logic opens up a world of possibilities in unary, binary and ternary based input systems [1]. Theoretically, MVL has the potential of improving circuit performance for applications, such as arithmetic and digital signal processing. Ternary based circuits are faster, require fewer operations, less gates, and signal lines. We have used MOSFETs due to the fact that MOSFETs support three levels which are required for ternary. The idea for a 1=2 gate design comes from a probabilistic implication of using three input data types to obtain an equal number of output types. In comparison to the 4 gate design limit imposed by permutation for binary gate design; a ternary system gives us the opportunity to realize 27 gates.

The current gate designs available are nothing but modified facsimiles of binary universal gates; namely the AND, OR, NAND, NOR and Inverter. The unique trit specific logical truth tables such as 1=2 Gate design have not been implemented; thus there is a need to create such gates so that we may be able to implement speedy ternary based combinational circuits.

TERNARY LOGIC

Ternary logic functions are defined as those functions having significance if a third value is introduced to the binary logic. In this paper, 0, 1, and 2 denote the ternary values to represent false, undefined, and true, respectively. Any n variable $\{X_1,...,X_n\}$ ternary function f (X) is defined as a logic function mapping $\{0,1,2\}$ n to $\{0, 1, 2\}$, where X $\{X_1,...,X_n\}$. The basic operations of ternary logic can be defined as follows, where

$X_i, X_j = \{0, 1, 2\}$ [13]:

$X_i + X_j = \max\{X_i, X_j\}$

$X_i \bullet X_j = \min\{X_i, X_j\}$

$X_i` = 2 - X_i$

where the operations +,•,` and are referred to as the OR, AND, and NOT in ternary logic, respectively. The fundamental gates in the design of digital systems are the inverter, the NOR gate, and the NAND gate. The assumed logic symbols are shown in Table I. The ternary gates are designed according to the convention defined by (1).

Table 1

Voltage (V)	Symbol
-5	0
0	1
5	2

BLOCK DIAGRAM AND WORKING PRINCIPLE
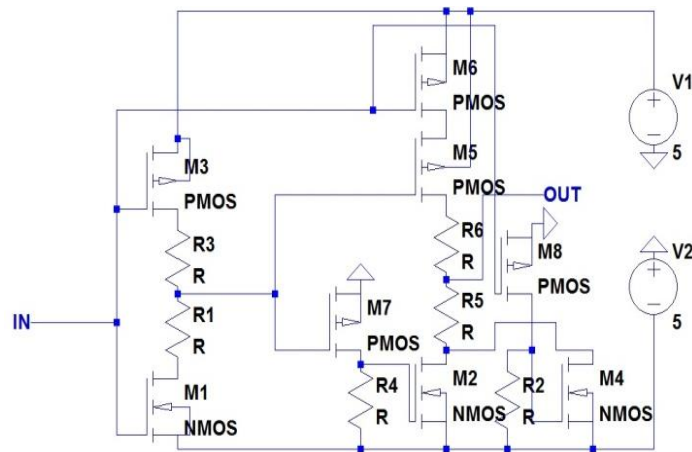
Figure 1: 1=2 Logic Gates

Table 2: Truth Table of 1=2

A	A*
0	0
1	2
2	0

REDUCING STATE CIRCUITS

M7, M2 and R4 form the locking circuit

This circuit is used to reduce the possible states. The input to the gate of M2 is given from the junction of M7 and R4. When the gate of M7 is less than 0 V then the output on the gate of M2 will be 0 V. While when the voltage is greater than or equal to 0 V, the output will be -5V on the gate of M2. Therefore the only possible inputs to M2 are 0V and -5V. This will help us reduce possible states on the M2 mosfet. This is the crucial concept for 1 equal to 2 circuits.

Case 1: When the voltage at the gate of m7 is greater than 0V. Since the Vg>0, the p-type mosfet will not conduct and therefore the -5V will be provided at the gate of M2 through the resistor R4.

Case 2: When the voltage at the gate of M7 is less than 0V.

Since the Vg<0, the p-type mosfet will conduct and therefore the 0V will be provided at the gate of M2.

Table 3

Input at Gate M7 (V)	Input at Gate M2 (V)
5	-5
0	-5
-5	0

From the table 3 we can see that from all the 3 possible states, the states are reduced to just 2, therefore making the implementation of 1 equal to 2 possible.

Similarly the M4, M8 and R2 form the reducing state circuit also.

Working of 1=2

M1 and M3 take up the trits present in at the input and produce an antithetical output. The complimented output will be further used in the next stage.

In the second stage, M7 and M8 form the activation gates for M2 and M4. A gate voltage of 0V is applied to M2 and M4 when the gate voltage of M7 and M8 is less than 0V. All these gates together perform the 1 equal 2 operations.

For e.g when A = -5V, M5 and M6 is off. M8 is activated therefore M4 is activated. M7 and M2 is deactivated, therefore the output is -5V

When A=0V, M5 and M6 is activated. There M2, M7, M4 and M8 are deactivated and therefore the output is 5V which is the required output.

The values of the resistors are R=R1=R2=R3=R4=R5=R6= 50 kΩ. (kilo-ohm)

IMPLEMENTATION

The above circuits have been implemented and simulated in LTSpice.

APPLICATIONS

This is one of the most important gate and building block for other combinational circuit they can be implemented to make other ternary circuits. These along with 'Shift Up Shift Down Gates' can give us any set of outputs necessary. They can be used to realize asynchronous circuits[2]

FUTURE SCOPE

Since the data usage by simple as well as complex circuitry goes on increasing, we are reaching a point where the limitations of Moores law become self apparent. Hence there is an immediate real world need to replace our 'bit' based systems with the 'trit' based system. The use of these gates is to build the combinational circuits required to build a ternary ALU. The combinational circuits which will be built are multiplexer, demultiplexer, adder, sub tractor, encoder, decoder and various other needful circuits for the ALU.

CONCLUSIONS

Using 1=2 gate, Shift Up and Shift Down gate we can replicate all the possible Truth Tables. We can conclude that 1=2 gate facilitates us to make other complex combinational and sequential circuits. This is the fundamental building block for a ternary ALU.

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